## REMARKS

Claims 1-14 are pending and have been rejected by the Examiner. In view of the foregoing amendments and following remarks, Applicants respectfully request reconsideration of the application.

### Claim Objections

In paragraph two of the March 13, 2003 non-final Office Action, the Examiner objected to claims 3, 5, and 12 for not referring to a plural form of "barrel shift registers." Applicants thank the Examiner for noting these typographical errors. Appropriate amendments have been made to put the aforementioned claims in condition for allowance.

### Rejections Under 35 U.S.C. §102

In paragraph four of the March 13, 2003 non-final Office Action, the Examiner rejected claims 1, 7, 9, and 11-14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,308,189 to Nguyen (hereinafter referred to as *Nguyen*). Applicants respectfully traverse.

*Nguyen* discloses an apparatus and method for performing partial logical shifts of a multiple-word logical signal as implemented within a central processing unit. Note that FIG. 3 of *Nguyen* is a vector word shift mechanism contained within VMX unit 206 of FIG. 2 (column 3, lines 63-65). VMX unit 206 is part of CPU 110 (see FIG. 2 and column 3, lines 42-45). Portions of an

input logical signal to be shifted are input to a plurality of barrel shifters. Each barrel shifter performs a rotation of its associated input portion (col. 3, line 66 – col. 4, line 8). Each corresponding rotated portion output therefrom is masked with a preselected mask having m trailing zero bits, for a left shift, or m leading zero bits, for a right shift. Rotated portions from barrel shifters succeeding, for a left shift, or preceding, for a right shift, the barrel shifter associated with the corresponding rotated portion are masked with a complementary mask and logically combined with the masked rotated portion from the corresponding barrel shifter to form a corresponding portion of the shifted output signal (Abstract).

Amended claim 1 recites, in part, "... a second circuit *connected* to outputs from the first circuit and configured to send at least one received signal to at least one output endpoint ..." (emphasis added). *Nguyen* does not teach or disclose a second circuit connected to outputs from the first circuit. FIG. 3 of *Nguyen* shows each of the barrel shifters 301-304 coupled to a plurality of gates, inverters, and multiplexers. For example, barrel shifter 301 is connected to AND gate 314 and is further coupled to AND gates 335 and 322 through inverter 331. AND gates 335 and 322 are connected to multiplexer 337. In turn, multiplexer 337 and AND gate 314 are connected as inputs to OR gate 348 prior to reaching output 364. Output 364, in turn, is connected serially to load/store unit 208 and D-cache 212 before becoming available as an output on bus interface unit 214 (FIG. 2).

Therefore, *Nguyen* does not teach or disclose all of the limitations recited in amended claim 1. Specifically, the "second circuit" of the claimed invention is connected to outputs from the first circuit (having at least one pair of left and right barrel shift registers) and is further configured to send at least one received signal to at least one output endpoint. In contrast, *Nguyen* contains several intermediary circuits prior to an output signal being available. Applicants therefore respectfully submit that claim 1 is not anticipated by *Nguyen* and is in condition for allowance. Claims 2-6 and 12-13 depend, directly or indirectly, from claim 1 and are therefore allowable for at least the same reasons.

Amended claim 7 recites, in part, "... the plurality of multiplexers being selectably *connected* to the barrel shift registers ..." (emphasis added). As is shown with claim 1, *Nguyen* does not teach or disclose a plurality of multiplexers being selectably connected to the barrel shift registers. Therefore, *Nguyen* cannot anticipate claim 7. Claims 8-11 depend directly from claim 7 and are therefore allowable for at least the same reasons.

Amended claim 14 recites, in part, "...the plurality of multiplexers being selectably *connected* to the barrel shift registers ..." (emphasis added). As is shown with claim 1 above, *Nguyen* does not teach or disclose a plurality of multiplexers being selectably connected to the barrel shift registers. Therefore, *Nguyen* cannot anticipate claim 14.

Rejections Under 35 U.S.C. §103

In paragraph six of the March 13, 2003 non-final Office Action, the Examiner rejected claims 2, 3, 5, 6 and 10 under 35 U.S.C. §103(a) as being obvious in light of *Nguyen*. Applicants respectfully traverse this rejection. Claims 2, 3, 4, and 6 depend from amended claim 1. As has been shown, *Nguyen* does not anticipate amended claim 1. Therefore, claim 1 and any dependent claims must be found to be allowable. Further, since claim 10 depends from claim 7, claim 10 is allowable for at least the same reasons as put forth for claim 7, supra.

In paragraph seven of the March 13, 2003 non-final Office Action, the Examiner rejected claims 4 and 8 as being unpatentable over *Nguyen* in view of U.S. Patent No. 4,512,018 to Phelps et al. (hereinafter, *Phelps*). *Nguyen* has already been shown to be an ineffectual reference, as it does not anticipate amended independent claims 1, 7, or 14. Therefore, *Nguyen* cannot not be used as a basis for an obviousness rejection. Further, since claims 4 and 8 depend from claims 1 and 7 respectively, claims 4 and 8 are allowable for at least the same reasons as shown above.

## Conclusion

Based on the above remarks, Applicants believe that the rejections in the Office Action of March 13, 2003 are fully overcome, and that the application is in condition for allowance. If the Examiner has questions regarding this case he is invited to contact the Applicants' undersigned representative at the number given below.

Respectfully submitted,

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Version with markings to show changes made

In the Claims:

1. (thrice amended) An electronic switching apparatus for flexibly interconnecting a plurality of signal endpoints, the apparatus comprising:

a first circuit [for] configured to receive[ing] at least one input signal from at least one input endpoint, the first circuit having at least one pair of barrel shift registers coupled to at least one of the at least one input endpoint and configured to [for] receive[ing] the at least one input signal, the first circuit further configured to shift[ing] and rotate[ing] the at least one input signal[,] and further configured to transmit[ting] at least one output signal; and

a second circuit [coupled] connected to outputs from the first circuit [for] and configured to send[ing] at least one received signal to at least one output endpoint.

2. (twice amended) The electronic switching apparatus of claim 1, wherein the at least one input signal comprises a data signal that is configured to be received in serial form, the data signal including a plurality of data channels interleaved therein.

3. (twice amended) The electronic switching apparatus of claim 2, wherein the second circuit further comprises at least one multiplexer configured to be selectably [coupled] connected to the at least one pair of barrel shift registers thereby effectively enabling digital signal switching simultaneously between the at least one input endpoint and the at least one output endpoint.

4. (twice amended) The electronic switching apparatus of claim 1, wherein the at least one input signal comprises a data signal that is configured to be received in parallel form and converted to serial form.

5. (twice amended) The electronic switching apparatus of claim 2, wherein the at least one pair of barrel shift registers is configured to interconnect[s] a plurality of received input signals at different times.

7. (thrice amended) A method for electronic signal coupling, the method comprising the steps of:

receiving a first set of digital signals, the received first set of digital signals being provided to at least one pair of barrel shift registers;

shifting and rotating the first set of digital signals; and

transmitting a second set of digital signals, the transmitted second set of digital signals being provided from a plurality of multiplexers, the plurality of multiplexers being selectably [coupled] connected to the barrel shift registers such that at least one signal selected in the first set of digital signals is selectably coupled for transmission in the second set of digital signals.

9. (twice amended) The method of claim 7, wherein a plurality of digital signals in the first set of digital signals [are] is transmitted as digital signals in the second set of digital signals separately at different times.

12. (twice amended) The electronic switching apparatus of claim 1, wherein the at least one pair of barrel shift registers are [is a] loadable barrel shift registers.

14. (twice amended) A system for electronic signal coupling comprising:

means for receiving a first set of digital signals, the received first set of digital signals being provided to at least one pair of barrel shift registers;

means for shifting and rotating the first set of digital signals; and

means for transmitting a second set of digital signals, the transmitted second set of digital signals being provided from a plurality of multiplexers, the plurality of multiplexers being selectably [coupled] connected to the barrel shift registers such that at least one signal selected in the first set of digital signals is selectably coupled for transmission in the second set of digital signals.